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File Edit View Tools Window Help

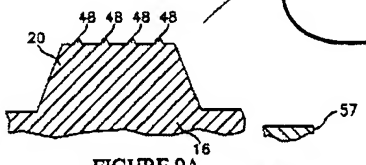


FIGURE 9A

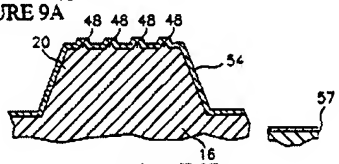


FIGURE 9B

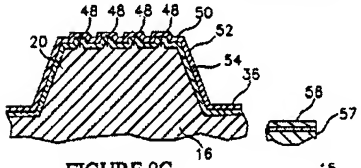


FIGURE 9C

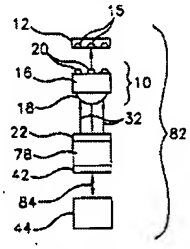


FIGURE 8

(FIG. 1). In addition, a membrane 18D physically and electrically connects the interconnect substrate 16 to test circuitry 44 substantially as previously described. The leveling mechanism 104A includes a leveling plate 110 and leveling screws 106A. As shown in FIG. 7F, three leveling screws 106A are arranged in a triangular pattern and threadably engage mating threaded openings in the leveling mechanism 104A. The leveling screws 106A permit the planarity of the contact members 20 to be adjusted with respect to a plane of the wafer 12 (FIG. 1). This allows the interconnect substrate 16 to be easily installed or replaced as required, without requiring the probe handler chuck to be replanarized. If desired the leveling screws 106A can be pivotably mounted to the leveling mechanism 104A using ball joints (not shown) or similar members.

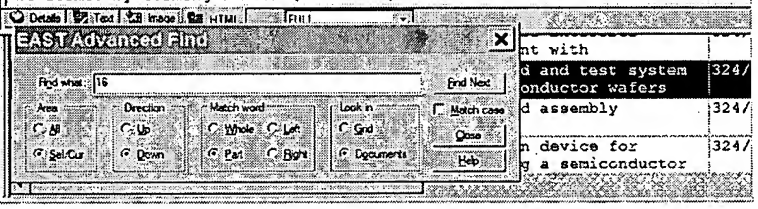
(43) Referring to FIG. 8, a system 82 constructed in accordance with the invention is shown. The system 82 includes a testing apparatus 78 in the form of a conventional wafer probe handler or similar apparatus. One suitable wafer probe handler is manufactured by Electroglass and is designated a Model 4080. The testing apparatus 78 is in electrical communication with or includes the test circuitry 44. The test circuitry 44 is adapted to send and receive test signals 84 for testing the integrated circuits on the wafer 12. The testing apparatus 78 can also include an optical or mechanical alignment system for aligning the contact locations 15 (FIG. 4) on the wafer 12 to the contact members 20 on the interconnect substrate 16.

(44) In addition, the testing apparatus 78 can include the pogo pins 42 in the conductive path from the test circuitry 44. The testing apparatus 78 can also include the probe card fixture 22. Still further, the testing apparatus 78 can include the force applying mechanism 32 for applying pressure to bias the interconnect substrate 16 against the wafer 12.

(45) The probe card 10 includes the membrane 18 and the interconnect substrate 16. The membrane 18 can be attached to the probe card fixture 22 as previously described. In addition, the interconnect substrate 16 can be attached to the membrane 18 also as previously described. The contact members 20 on the interconnect substrate are configured to penetrate the contact locations 15, on the wafer 12 to a limited penetration depth.

(46) Referring to FIGS. 9A-9C, a method for forming the raised contact members 20 using an etching process is shown. In the process illustrated in FIGS. 9A-9C, the interconnect substrate 16 comprises silicon or other etchable semiconductor material.

(47) Initially, as shown in FIG. 9A, the penetrating projections 48 can be formed by forming a mask (not shown) on the substrate 16 and then



* 16 comprises silicon ~~wafer~~ (of ~~wafer~~ 12)

* 20 pads

For 10/746031

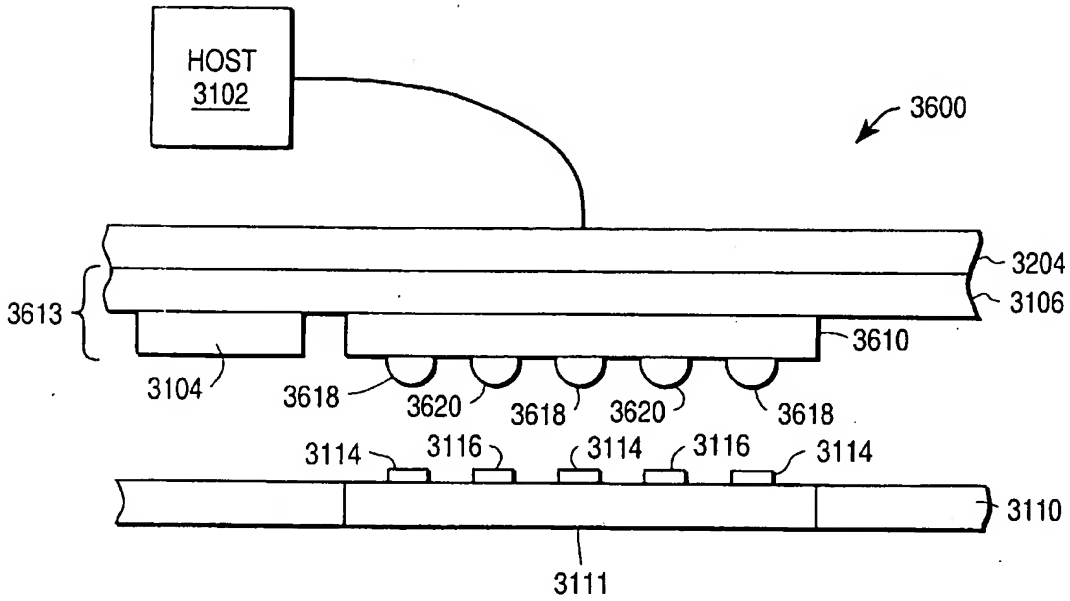


FIG. 36

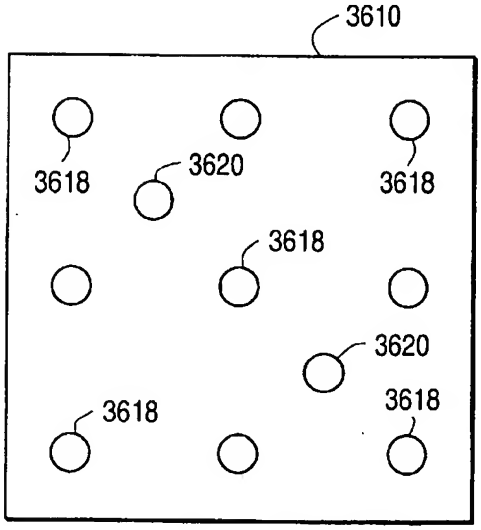


FIG. 37

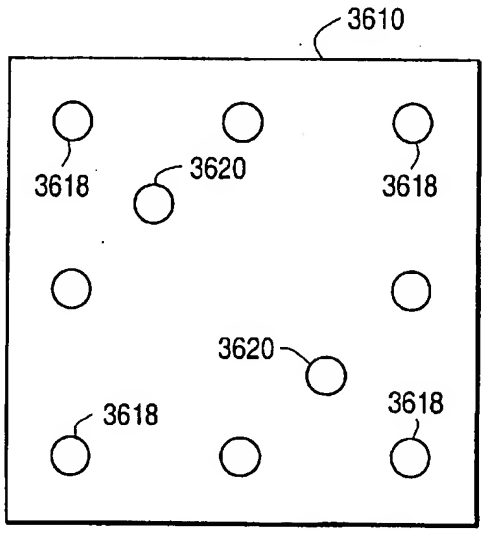


FIG. 38

FIG. 15

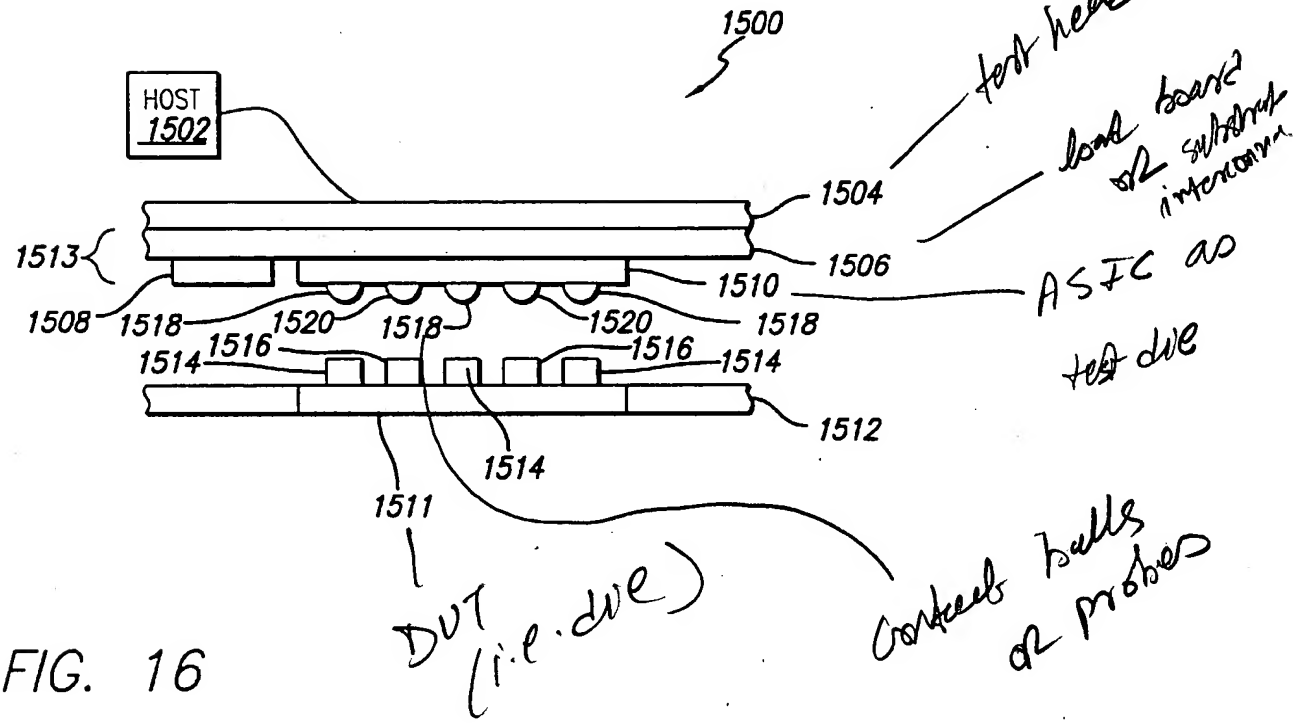


FIG. 16

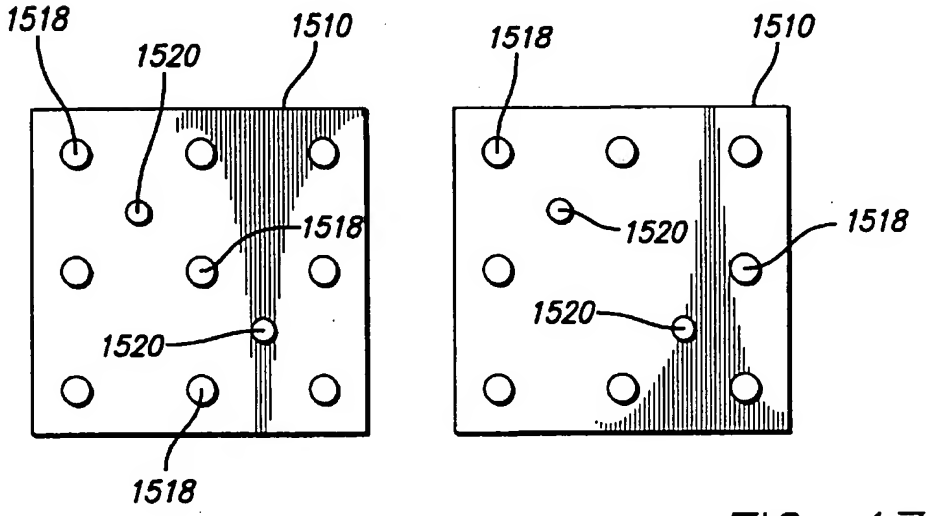


FIG. 17